IN THE CLAIMS

None of the claims are amended, canceled, or added. The claims are repeated herein only for reviewing convenience.

1. (Original) A method comprising:

delaying a first clock signal to produce a delayed clock signal;

measuring time intervals between phases of the first clock signal; and

adjusting the delayed clock signal based on the time intervals.

2. (Original) The method of claim 1, further comprising:

generating the first clock signal from an input clock signal, wherein the first clock signal includes first pulses, which correspond to leading edges of the input clock signal, and second pulses, which correspond to falling edges of the input clock signal.

3. (Original) The method of claim 2, wherein measuring the time intervals comprises:

determining a first duty cycle skew of the first clock signal by adjusting a time delay between the first clock signal and the delayed clock signal; and

comparing the first clock signal and the delayed clock signal.

4. (Original) The method of claim 3, wherein determining the first duty cycle skew comprises:

adjusting the time delay to a first value, which indicates a first time delay when a first delayed pulse of the delayed clock signal occurs in proximity to a second pulse of the first clock signal;

adjusting the time delay to a second value, which indicates a second time delay when a second delayed pulse of the delayed clock signal occurs in proximity to a first pulse of the first clock signal; and

determining the first duty cycle skew based on the first time delay and the second time delay.

5. (Original) The method of claim 3, wherein adjusting the delayed clock signal comprises:

producing a third clock signal with a second duty cycle skew, wherein the second duty cycle skew is less than the first duty cycle skew by a time difference that is based on the first duty cycle skew.

6. (Original) A method comprising:

generating a first clock signal from an input clock signal, wherein the first clock signal includes first pulses, which correspond to leading edges of the input clock signal, and second pulses, which correspond to falling edges of the input clock signal;

delaying the first clock signal by a time delay to produce a delayed clock signal having first delayed pulses and second delayed pulses;

determining a first duty cycle skew of the first clock signal by adjusting the time delay and comparing the first clock signal and the delayed clock signal; and

producing a third clock signal with a second duty cycle skew, wherein the second duty cycle skew is less than the first duty cycle skew by a time difference that is based on the first duty cycle skew.

7. (Original) The method of claim 6, wherein determining the first duty cycle skew comprises:

adjusting the time delay to a first value, which indicates a first time delay when a first delayed pulse of the delayed clock signal occurs in proximity to a second pulse of the first clock signal;

adjusting the time delay to a second value, which indicates a second time delay when a second delayed pulse of the delayed clock signal occurs in proximity to a first pulse of the first clock signal; and

determining the first duty cycle skew based on the first time delay and the second time delay.

8. (Original) The method of claim 6, wherein producing the third clock signal comprises:

calculating a skew adjustment value as approximately one half of a difference between

the first time delay and the second time delay; and

applying the skew adjustment value to a clock signal to produce the third clock signal.

9. (Original) An apparatus comprising:

a delay element, which functions to delay a first clock signal to produce a delayed clock signal;

a detector, operatively coupled to the delay element, which functions to measure time intervals between phases of the first clock signal based on comparisons between the first clock signal and the delayed clock signal; and

a control element, operatively coupled to the detector, which functions to adjust the delayed clock signal based on the time intervals.

10. (Original) The apparatus of claim 9, further comprising:

a clock generator, which functions to generate the first clock signal from an input clock signal, wherein the first clock signal includes first pulses, which correspond to leading edges of the input clock signal, and second pulses, which correspond to falling edges of the input clock signal.

11. (Original) The apparatus of claim 10, wherein the detector functions to measure the time intervals by:

determining a first duty cycle skew of the first clock signal by adjusting a time delay between the first clock signal and the delayed clock signal; and

comparing the first clock signal and the delayed clock signal.

12. (Original) An apparatus comprising:

a clock generator, which functions to generate a first clock signal from an input clock signal, wherein the first clock signal includes first pulses, which correspond to leading edges of the input clock signal, and second pulses, which correspond to falling edges of the input clock signal;

a delay element, operatively coupled to the clock generator, which functions to delay the

first clock signal by a time delay to produce a delayed clock signal having first delayed pulses and second delayed pulses; and

a first circuit, operatively coupled to the delay element, which functions to determine a first duty cycle skew of the first clock signal by adjusting the time delay and comparing the first clock signal and the delayed clock signal, and which further functions to provide control information for producing a third clock signal with a second duty cycle skew, wherein the second duty cycle skew is less than the first duty cycle skew by a time difference that is based on the first duty cycle skew.

13. (Original) The apparatus of claim 12, wherein the first circuit determines the first duty cycle skew by:

adjusting the time delay to a first value, which indicates a first time delay when a first delayed pulse of the delayed clock signal occurs in proximity to a second pulse of the first clock signal;

adjusting the time delay to a second value, which indicates a second time delay when a second delayed pulse of the delayed clock signal occurs in proximity to a first pulse of the first clock signal; and

determining the first duty cycle skew based on the first time delay and the second time delay.

14. (Original) The apparatus of claim 12, wherein the first circuit provides the control information by:

calculating a skew adjustment value as approximately one half of a difference between the first time delay and the second time delay; and

applying the skew adjustment value to a clock signal to produce the third clock signal.

15. (Original) A microprocessor comprising:

a delay element, which functions to delay a first clock signal to produce a delayed clock signal;

a detector, operatively coupled to the delay element, which functions to measure time

intervals between phases of the first clock signal based on comparisons between the first clock signal and the delayed clock signal; and

a control element, operatively coupled to the detector, which functions to adjust the delayed clock signal based on the time intervals.

16. (Original) The microprocessor of claim 15, further comprising:

a clock generator, which functions to generate the first clock signal from an input clock signal, wherein the first clock signal includes first pulses, which correspond to leading edges of the input clock signal, and second pulses, which correspond to falling edges of the input clock signal.

17. (Original) The microprocessor of claim 16, wherein the detector functions to measure the time intervals by:

determining a first duty cycle skew of the first clock signal by adjusting a time delay between the first clock signal and the delayed clock signal; and

comparing the first clock signal and the delayed clock signal.

18. (Original) A microprocessor comprising:

a clock generator, which functions to generate a first clock signal from an input clock signal, wherein the first clock signal includes first pulses, which correspond to leading edges of the input clock signal, and second pulses, which correspond to falling edges of the input clock signal;

a delay element, operatively coupled to the clock generator, which functions to delay the first clock signal by a time delay to produce a delayed clock signal having first delayed pulses and second delayed pulses; and

a first circuit, operatively coupled to the delay element, which functions to determine a first duty cycle skew of the first clock signal by adjusting the time delay and comparing the first clock signal and the delayed clock signal, and which further functions to provide control information for producing a third clock signal with a second duty cycle skew, wherein the second duty cycle skew is less than the first duty cycle skew by a time difference that is based on the

first duty cycle skew.

19. (Original) The microprocessor of claim 18, wherein the first circuit determines the first duty cycle skew by:

adjusting the time delay to a first value, which indicates a first time delay when a first delayed pulse of the delayed clock signal occurs in proximity to a second pulse of the first clock signal;

adjusting the time delay to a second value, which indicates a second time delay when a second delayed pulse of the delayed clock signal occurs in proximity to a first pulse of the first clock signal; and

determining the first duty cycle skew based on the first time delay and the second time delay.

20. (Original) The microprocessor of claim 18, wherein the first circuit provides the control information by:

calculating a skew adjustment value as approximately one half of a difference between the first time delay and the second time delay; and

applying the skew adjustment value to a clock signal to produce the third clock signal.